wider than the silicon oxide band gap, then the second oxide layer 216 is left out. Alternately, if the band gap of the high dielectric constant dielectric layer 214 is less than the silicon oxide band gap, then the second oxide layer 216 is included. Table 2 below indicates the band gap values of the utilized dielectric layer 214 material in the present embodiment and furthermore includes the band gap values of SiO_2 and Si_3N_4.

[0026] As shown in Tables 1 and 2, the Al_2O_3 band gap is greater than the Si_3N_4/SiO_2 band gap. Since the Al_2O_3 band gap is similar to the SiO_2 band gap, when using Al_2O_3 as the material of the dielectric layer 214, the other oxide layers 212 and 216 within the dielectric stacked layer 210 are replaced, thereby simplifying the manufacturing process of the flash memory.

FOR THE CLAIMS:

Please cancel claim 3 without prejudice or disclaimer.

Please substitute the claim with the following claim with the same numbering.

1. (Once Amended) A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;

a high dielectric constant dielectric layer located upon the first oxide layer, wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8;

a second oxide layer, located upon the high dielectric constant dielectric layer, wherein,

together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;

a control gate formed on the second oxide layer of the dielectric stacked layer; and

a source/drain region located in the substrate on the two sides of the floating gate.

7. (Once Amended) A flash memory structure, comprising:

a tunneling ~~oxide layer~~ located upon a substrate;

a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;

a high dielectric constant dielectric layer having a dielectric constant greater than 8 located upon the first oxide layer, wherein, together with the oxide layer, a dielectric stacked layer is formed;

a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and

a source/drain region located within the substrate on the two sides of the floating gate.